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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/806,680	03/22/2004	Narain D. Arora	700693-4026	1158

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EXAMINER	
LIN, SUN J	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 11/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/806,680	ARORA ET AL.	
	Examiner	Art Unit	
	Sun J. Lin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19 and 21-30* is/are rejected.

7)☒ Claim(s) *20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03/22/2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/22/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/806,680 filed on 03/22/2004. Claims 1 – 30 remain pending in the application.

Drawing Objections

2. Drawings are objected to because of following informalities:

Fig. 2B delete item "Ground 205".
Fig. 4, meanings of dashed line connecting Vss G is not clear.
Due to poor hand writing, many labels shown in Fig. 1 – Fig. 4 are not readable.

Appropriate corrections are required.

Claim Objections

3. Claim listed below is objected to because of the following informalities:

Claim 1, line 5, after "first" insert —**conductor**—.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

5. Claims 11 – 19 and 21 – 30 are rejected under 35 U.S.C. 102(a) as being unpatentable over IEEE Paper entitled " Non-Destructive Inverse Modeling of Copper Interconnect Structure for 90nm Technology Node" authored by *Kunikiyo et al.*

6. As to Claim 11, *Kunikiyo et al.* disclose the following subject matter:

- Charge-based capacitance measurement (CBCM) method for use in determining coupling capacitances of a test structure within an integrated circuit, the test structure comprising a upper metal plate (i.e., first plate), a lower metal plate (i.e., second plate), a first conductor and a second conductor that are formed as a *comb-like structure* are disposed between the upper metal plate and the lower metal plate – [Fig. 1; Fig. 2; Section I; Section II];
- Determining a capacitance C_{up} (i.e., first capacitance) between the upper metal plate (first plate) and the first conductor or the second conductor – [Fig. 2; Section II];
- Determining a capacitance C_{low} (i.e., second capacitance) between the lower metal plate (second plate) and the first conductor or the second conductor – [Fig. 2];
- Determining a capacitance C_c (i.e., third capacitance) between the first conductor and the second conductor – [Fig. 2; Section II].

For reference purposes, the explanations given above in response to Claim 11 are called **[Response A]** hereinafter.

7. As to Claim 22, in addition to reasons included in **[Response A]** given above, *Kunikiyo et al.* shows in Fig. 1, a current measurement circuit, which is in electrical communication with first conductor and second conductor in the comb-like structure, in CBCM test structure for use in measuring coupling capacitance C_C between the first conductor and the second conductor. Notice that a current measurement circuit can be in electrical communication with upper metal plate (first conductive plate) and the first conductor or the second conductor to measurement C_{up}, and a current measurement circuit can be in electrical communication with lower metal plate (second conductive plate) and the first conductor or the second conductor to measurement C_{low}.

8. As to Claims 12 and 23, *Kunikiyo et al.* disclose subject matter regarding (1) non-destructive inverse modeling of copper interconnect cross-sectional structure – [abstract] (2) test structure measuring the intra- and interlayer coupling capacitance

parasitic to copper interconnects – [Section II]. Notice that the upper metal layer (first plate) and the lower metal layer (second plate) can be made of copper.

9. As to Claims 13 and 22, the shapes of first conductor and the second conductor in the comb-line structure are symmetrical – [Fig. 1].

10. As to Claim 14 and 25, reasons (comb-link test structure) are included in **[Response A]** given above.

11. As to Claims 15, 16, 26 and 27, measurement method proposed by *Kunikiyo et al.* can be applied to a test structure having a first conductor and a second conductor of any symmetrical shape, including maze shape and serpentine shape.

12. As to Claims 17, 18, 28 and 29, both the upper metal plate (first plate) and the lower metal plate (second plate) can be solid plates or slotted plates as long as an equipotential is existing at anywhere on each of the "plates".

13. As to Claim 19, due to small dimensions of test structure built on a test wafer in 90nm technology, it is well known in the art that a probe station interfaced with an Agilent Precision LCR meter 4284A is utilized for capacitance measurement. Notice that, for achieving accurate measurement, a set of standard probe pads, which are in electrical communication with upper metal plate, lower metal plate, first conductor and second conductor, respectively.

14. As to Claims 21and 30, due to capacitances are determined through measurements, a cross-section of the first conductor can be non-rectangular and a cross-section of the second conductor can be non-rectangular.

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

(1). Determining the scope and contents of the prior art.
(2). Ascertaining the differences between the prior art and the claims at issue.
(3). Resolving the level of ordinary skill in the pertinent art.
(4). Considering objective evidence present in the application indicating obviousness or nonobviousness.

16. Claims 1 – 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over IEEE Paper entitled " Non-Destructive Inverse Modeling of Copper Interconnect Structure for 90nm Technology Node" authored by *Kunikiyo et al.* in view of U.S. Patent No. 6,312,963 B1 to *Chou et al.*

17. As to Claim 1, *Kunikiyo et al.* disclose the following subject matter:

- Using Charge-based capacitance measurement (CBCM) method in determining a (first) set of coupling capacitances (C_{up}, C_{low} and C_C) associated with a comb-line test structure for use in determining process parameters of an integrated circuit – **[Response A]**.

Kunikiyo et al. do not teach a method of using a field solver in calculating a (second) set of coupling capacitance associated with a test structure for use in determining the process parameters. But *Chou et al.* teach a method of using a field solver to accurately predict interconnect process parameters – [abstract]. *Chou et al.* also teach the following subject matter:

- Given an actually measured (coupling) capacitance of a test structure, the interconnect process parameters can be obtained by successive approximation... successively refined approximations of the interconnect process parameter of interest are fed into field solver until the filed solver predicts, within predetermined tolerance limits, the measured capacitance... The current approximation of interconnect process parameter when the predicted

value converges to the measured value is the desired value for the interconnect process parameter – [col. 9, line 16 – 28].

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have applied the teachings of *Chou et al.* in numerically calculating a second set of coupling capacitances associated with the test structure in order to successively refine approximations of the interconnect process parameters thereby achieving a correct value for the interconnect process parameters.

For reference purposes, the explanations given above in response to Claim 1 are called **[Response B]** hereinafter.

18. As to Claims 2 and 6, reasons are included in **[Response B]** given above,

19. As to Claim 3, in addition to reasons included in **[Response B]** given above, *Chou et al.* teach previous approximations of interconnect process parameters of interest are successively fed into field solver to successively predict next approximations of the interconnect parameters until a desired and accurate values of interconnect process parameters are obtained. Therefore, at the beginning of approximation process, initial process parameters are inputted into the field solver.

20. As to Claims 4 and 5, *Chou et al.* teach the following subject matter in – [col. 4, line 26 – col. 5, line 5; col. 8, line 59 – col. 9, line 28].

21. As to Claims 7 and 8, *Kunikiyo et al.* disclose (1) comb-like copper interconnect test structure containing a first copper conductor and a second copper conductor – [Section II, Fig. 1] (2) upper metal plate, lower metal plate, interconnects – [Fig. 2]; Notice that the upper metal layer (first plate) and the lower metal layer (second plate) can be made of copper.

22. As to Claim 9, *Kunikiyo et al.* show and disclose the subject matter (CBCM circuit) in Fig. 1.

23. As to Claim 10, *Chou et al.* disclose that a cross-section of the test structure is a trapezoidal (i.e., non-rectangular) – [col. 5, line 30 – 45].

Allowable Subject Matter

24. Claim 20 is objected to as being dependent upon a rejected base claim, but it would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Those claims are allowed is because that the prior art does not teach or fairly suggest the following subject matter:

- A method for determining coupling capacitance of a test structure within an integrated circuit wherein a first plate is in electrical communication with a first multiplexer, a second conductor is in electrical communication with a second multiplexer, a second conductor is in electrical communication with a third multiplexer, a second plate is in electrical communication with a fourth multiplexer in combination with other limitations as recited in independent **Claim 20.**

Conclusion

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sun J Lin whose telephone number is (571) 272 - 1899. The examiner can normally be reached on Monday-Friday 9:30AM - 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on (571) 272 - 1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sun James Lin
Patent Examiner
Art Unit 2825
November 25, 2005